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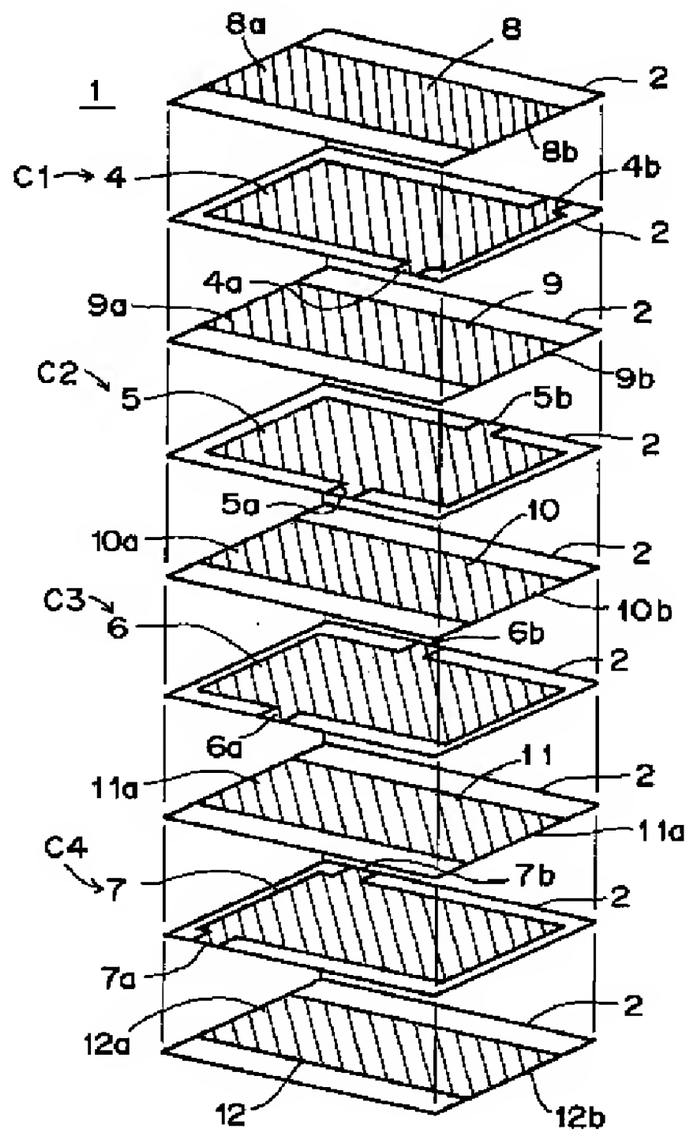
(54)【発明の名称】　貫通型積層コンデンサアレイ

(57)【要約】
【課題】　コンデンサ素子間のクロストークが少なく、かつ、小型で大容量の貫通型積層コンデンサアレイを得る。
【解決手段】　貫通型積層コンデンサアレイ１は、貫通電極４，５，６，７をそれぞれ表面に設けた誘電体シート２と、グランド電極８，９，１０，１１，１２をそれぞれ表面に設けた誘電体シート２等にて構成されている。貫通電極４～７は積層方向に異なる位置に配置され、貫通コンデンサ素子Ｃ１～Ｃ４は積層方向に積み重ねられた構造になっている。



【特許請求の範囲】
【請求項１】　複数の貫通電極と複数のグランド電極と複数の誘電体層を積層して構成した、複数の貫通コンデンサ素子を有した貫通型積層コンデンサアレイにおいて、
前記複数の貫通電極をそれぞれ積層方向に異なる位置に配設して前記複数の貫通コンデンサ素子の位置をそれぞれ積層方向に異ならせたことを特徴とする貫通型積層コンデンサアレイ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、貫通型積層コンデンサアレイ、特に、高周波領域で用いられる貫通型積層コンデンサアレイに関する。
【０００２】
【従来の技術】従来の貫通型積層コンデンサアレイは、例えば図５に示すように、四つの貫通電極３２を表面に並設した誘電体シート３１を、グランド電極３４を表面に設けた２枚の誘電体シート３１にて挟み、さらにこの上下両側に保護層用誘電体シート（図示せず）を配設して積層体３６とする。積層体３６の表面には、図６に示すように、信号外部電極３８ａ～３８ｄ，３９ａ～３９ｄ及びグランド外部電極４０，４１が形成され、貫通型積層コンデンサアレイ４３とされる。
【０００３】図７はこのコンデンサアレイ４３の電気等価回路図である。それぞれの貫通電極３２はグランド電極３４と共に、四つの貫通コンデンサ素子Ｃ１～Ｃ４を構成している。そして、これらの貫通コンデンサ素子Ｃ１～Ｃ４は、積層方向に等しい位置に配設されている。
【０００４】
【発明が解決しようとする課題】従来のコンデンサアレイ４３にあっては、隣接する貫通電極３２間に浮遊容量Ｃｓが発生し易く、そのため、貫通電極３２間での電磁干渉、いわゆるクロストークが発生し易い。特に、コンデンサアレイが、高周波領域で用いられる際にクロストークの問題は顕著になる。
【０００５】このクロストークの対策として、図８に示すように、貫通電極３２の間隔を十分確保したり、図９に示すように、貫通電極３２間にグランド電極４５を配設する等の対策が考えられる。しかし、部品サイズが同一であれば静電容量が小さくなり、同一の容量を得ようとすれば部品サイズが大きくなるという不具合がある。
【０００６】そこで、本発明の目的は、コンデンサ素子間のクロストークが少なく、かつ、小型で大容量の貫通型積層コンデンサアレイを提供することにある。
【０００７】
【課題を解決するための手段】以上の目的を達成するため、本発明に係る貫通型積層コンデンサアレイは、複数の貫通電極をそれぞれ積層方向に異なる位置に配設して複数の貫通コンデンサ素子の位置をそれぞれ積層方向に異ならせたことを特徴とする。
【０００８】
【作用】以上の構成により、貫通コンデンサ素子の配設位置が積層方向に異なる構造となり、それぞれの貫通コンデンサ素子の貫通電極間に配設されたグランド電極が貫通電極相互間に発生する浮遊容量を抑える。
【０００９】
【発明の実施の形態】以下、本発明に係る貫通型積層コンデンサアレイの一実施形態について添付図面を参照して説明する。なお、本実施形態は、四つの貫通コンデンサ素子を備えたものについて説明するが、これ以外に二つ、三つ、あるいは五つ以上の貫通コンデンサ素子を備えたものであってもよいことは言うまでもない。
【００１０】図１に示すように、貫通型積層コンデンサアレイ１は、貫通電極４，５，６，７をそれぞれ表面に設けた誘電体シート２と、グランド電極８，９，１０，１１，１２をそれぞれ表面に設けた誘電体シート２と、保護層用誘電体シート（図示せず）等にて構成されている。誘電体シート２の材料としては、エポキシ等の樹脂あるいはセラミック誘電体等が用いられる。
【００１１】貫通電極４は、誘電体シート２の表面に広面積に形成され、二つの引出し部４ａ，４ｂを有している。引出し部４ａは誘電体シート２の手前側の辺の右側の位置に露出し、引出し部４ｂはシート２の奥側の辺の右側の位置に露出している。同様にして、貫通電極５は、誘電体シート２の表面に広面積に形成され、引出し部５ａはシート２の手前側の辺の中央部右寄りの位置に露出し、引出し部５ｂはシート２の奥側の辺の中央部右寄りの位置に露出している。貫通電極６はシート２の表面に広面積に形成され、引出し部６ａはシート２の手前側の辺の中央部左寄りの位置に露出し、引出し部６ｂはシート２の奥側の辺の中央部左寄りの位置に露出している。貫通電極７はシート２の表面に広面積に形成され、引出し部７ａはシート２の手前側の辺の左側の位置に露出し、引出し部７ｂはシート２の奥側の辺の左側の位置に露出している。各貫通電極４～７は同一形状をしているが、必ずしもこれに限定するものではなく、異なる形状であってもよい。
【００１２】グランド電極８～１２はそれぞれ誘電体シート２の表面に広面積に形成され、それぞれの引出し部８ａ，９ａ，１０ａ，１１ａ，１２ａはシート２の左辺に露出し、引出し部８ｂ，９ｂ，１０ｂ，１１ｂ，１２ｂはシート２の右辺に露出している。電極４～１２はＡｇ－Ｐｄ，Ａｇ，Ｐｄ，Ｃｕ等の材料からなり、スパッタリング法、真空蒸着法、印刷法等の方法により形成される。
【００１３】各誘電体シート２は、貫通電極４～７をそれぞれ設けた誘電体シート２とグランド電極８～１２をそれぞれ設けた誘電体シート２を交互に積み重ねた後、上下両側に保護層用誘電体シートを配設し、一体的に焼

結することにより、図２に示すように積層体とされる。図３に示すように、積層体の左右の側面部にはグランド外部電極１７，１８が形成され、手前側の側面部には等間隔で入力外部電極１５ａ，１５ｂ，１５ｃ，１５ｄが形成され、奥側の側面部には等間隔で出力外部電極１６ａ，１６ｂ，１６ｃ，１６ｄが形成されている。外部電極１５ａ～１５ｄ，１６ａ～１６ｄ，１７，１８はスパッタリング法、真空蒸着法、塗布法等の方法により形成され、Ａｇ－Ｐｄ，Ａｇ，Ｐｄ，Ｃｕ等の材料からなる。

【００１４】入力外部電極１５ａ～１５ｄはそれぞれ貫通電極４～７の引出し部４ａ～７ａに電気的に接続され、出力外部電極１６ａ～１６ｄはそれぞれ貫通電極４～７の引出し部４ｂ～７ｂに電気的に接続され、外部グランド電極１７，１８はそれぞれグランド電極８～１２の引出し部８ａ～１２ａ，８ｂ～１２ｂに電気的に接続されている。

【００１５】こうして得られたコンデンサアレイ１は、グランド電極８，９と貫通電極４とで貫通コンデンサ素子Ｃ１を構成し、グランド電極９，１０と貫通電極５とで貫通コンデンサ素子Ｃ２を構成し、グランド電極１０，１１と貫通電極６とで貫通コンデンサ素子Ｃ３を構成し、グランド電極１１，１２と貫通電極７とで貫通コンデンサ素子Ｃ４を構成している。すなわち、グランド電極９，１０，１１は隣接する貫通コンデンサ素子に共有されている。図４はコンデンサアレイの電気等価回路図である。

【００１６】このコンデンサアレイ１において、貫通電極４～７は積層方向、すなわち電極４～７の厚み方向に異なる位置に配置され、貫通コンデンサ素子Ｃ１～Ｃ４は積層方向に積み重ねられた構造になっている。貫通電極４と５の間にはグランド電極９が配設されているので、これによって貫通電極４と５間に発生する浮遊容量が抑えられ、貫通コンデンサ素子Ｃ１とＣ２間のクロストークが発生しにくくなる。同様にして、貫通電極５と６間に発生する浮遊容量は、グランド電極１０によって抑えられ、貫通コンデンサ素子Ｃ２とＣ３間のクロストークが発生しにくくなる。貫通電極６と７間に発生する浮遊容量は、グランド電極１１によって抑えられ、貫通コンデンサ素子Ｃ３とＣ４間のクロストークが発生しにくくなる。

【００１７】また、貫通電極４～７やグランド電極８～１２を積層する構造であるため、同一層には１電極しか配設されず、これらの電極４～１２を広面積に設定することができ、大容量の静電容量が得られる。しかも、同一誘電体シート上に並置された貫通電極の間隔を十分確保したり、あるいは同一誘電体シート上に並置された貫通電極間にグランド電極を配設する構造ではないので、部品サイズが小型となり、プリント基板等に占める面積が小さくてすむ。

【００１８】なお、本発明に係る貫通型積層コンデンサアレイは前記実施形態に限定するものではなく、その要旨の範囲内で種々に変更することができる。前記実施形態の各貫通コンデンサ素子は１つの貫通電極と２つのグランド電極にて構成されているが、静電容量を大きくするために貫通電極とグランド電極の枚数を増やしてもよい。また、隣接する貫通コンデンサ素子は、グランド電極を共有しているが、各貫通コンデンサ素子毎に独立したグランド電極を有するものであってもよい。

【００１９】さらに、前記実施形態は個産品の場合を例にして説明したが、量産時の場合には複数個のコンデンサアレイを備えたマザー基板にて製作し、所望のサイズに切り出して製品とすることができる。また、前記実施形態は、シートを積み重ねた後、一体的に焼成するものであるが、必ずしもこれに限定されない。シートは予め焼結されたものを用いてもよい。また、印刷等の方法によりペースト状の誘電体材料や導電体材料を順に塗布、乾燥して重ね塗りすることによって、積層構造を有するコンデンサアレイを得てもよい。

【００２０】

【発明の効果】以上の説明で明らかなように、本発明によれば、貫通電極を積層方向に異なる位置に配置して貫通コンデンサ素子の位置をそれぞれ積層方向に異ならせたので、積層方向に配置された貫通電極間にグランド電極が配設され、このグランド電極が貫通電極相互間に発生する浮遊容量を低減させる。この結果、コンデンサ素子間のクロストークが少なく、小型で大容量の貫通型積層コンデンサアレイが得られる。

【図面の簡単な説明】

【図１】本発明に係る貫通型積層コンデンサアレイの一実施形態を示す分解斜視図。

【図２】図１に示した貫通型積層コンデンサアレイの積層状態を示す斜視図。

【図３】図１に示した貫通型積層コンデンサアレイの外観を示す斜視図。

【図４】図３に示した貫通型積層コンデンサアレイの電気等価回路図。

【図５】従来の貫通型積層コンデンサアレイの分解斜視図。

【図６】図５に示した貫通型積層コンデンサアレイの外観を示す斜視図。

【図７】図６に示した貫通型積層コンデンサアレイの電気等価回路図。

【図８】従来の貫通電極層の変形例を示す斜視図。

【図９】従来の貫通電極層の別の変形例を示す斜視図。

【符号の説明】

１…貫通型積層コンデンサアレイ

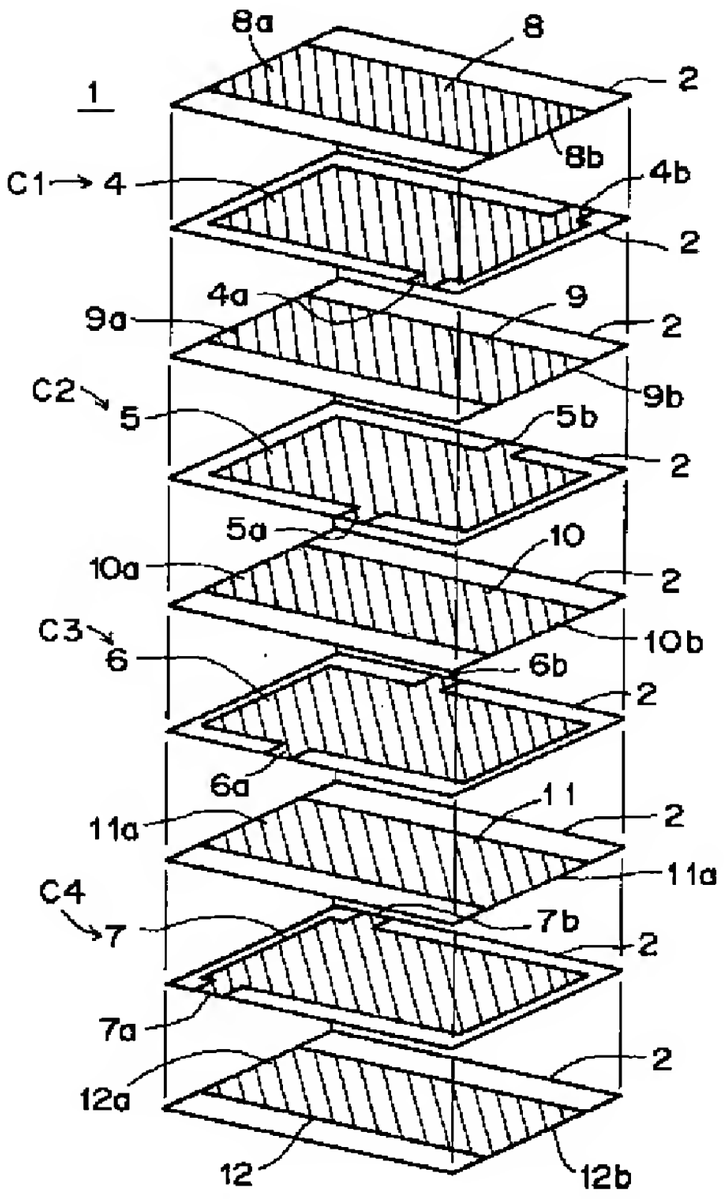
２…誘電体シート

４，５，６，７…貫通電極

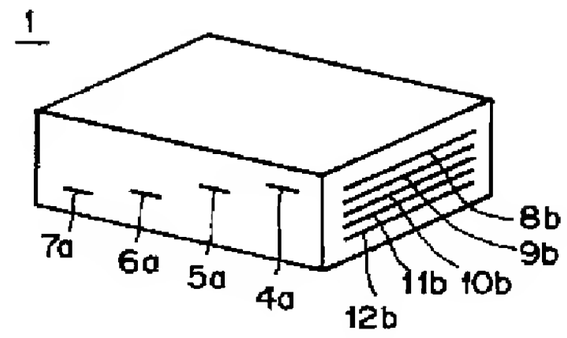
８，９，１０，１１，１２…グランド電極

Ｃ１，Ｃ２，Ｃ３，Ｃ４…貫通コンデンサ素子

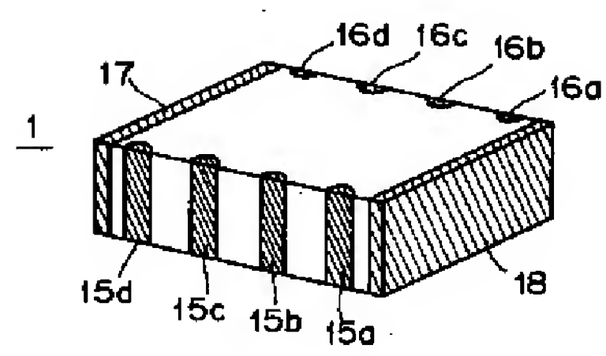
【図１】



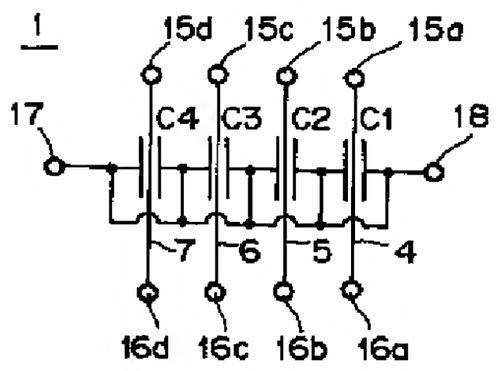
【図２】



【図３】



【図４】



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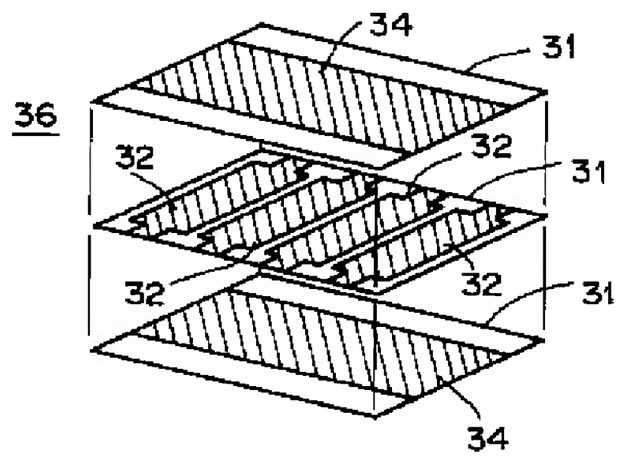
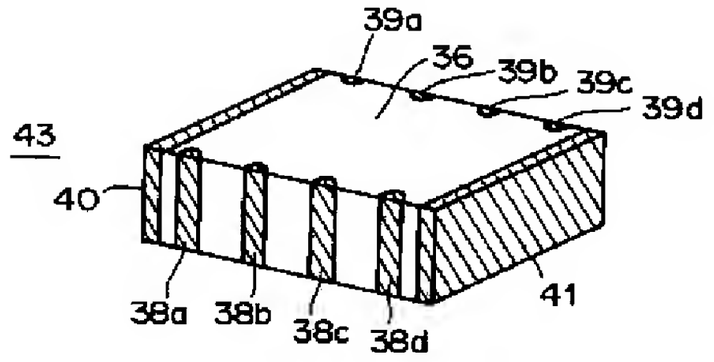


【図６】



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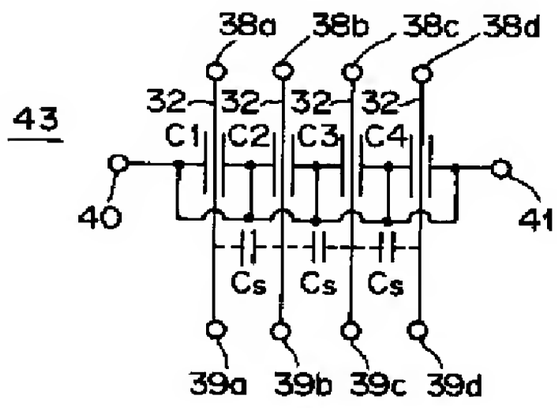
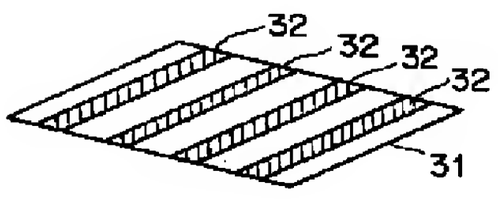
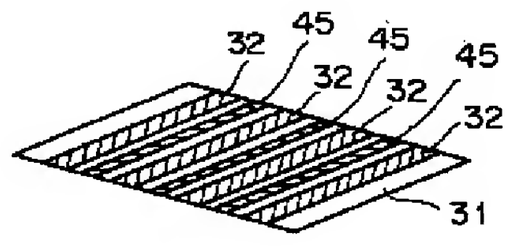


【図８】



【図９】



PATENT ABSTRACTS OF JAPAN

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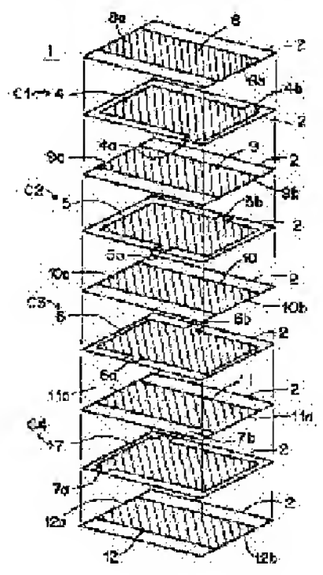
KAWAGUCHI YOSHIO

(54) THROUGH-TYPE LAYER-BUILT CAPACITOR ARRAY



(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a small size and large capacity through-type layer/built capacitor array in which there is little crosstalk between capacitor elements.

SOLUTION: A through-type layer-built capacitor array 1 is comprised of dielectric sheets 2 on which through electrodes 4, 5, 6 and 7 are respectively formed, dielectric sheets 2 on which grounding electrodes 8, 9, 10, 11 and 12 are

respectively formed, etc. The through electrodes 4-7 are provided at different positions in a layer-building direction and through-type capacitor elements are piled on a layer-building direction.

LEGAL STATUS

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[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

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[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]

[Claim 1] The penetration mold multilayer capacitor array characterized by having arranged said two or more penetration electrodes in a location which is different in the direction of a laminating, respectively in the penetration mold multilayer capacitor array with two or more feedthrough capacitor components which carried out the laminating of two or more penetration electrodes, two or more grand electrodes, and two or more dielectric layers, and constituted them, and changing the location of two or more of said feedthrough capacitor components in the direction of a laminating, respectively.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a penetration mold multilayer capacitor array and the penetration mold multilayer capacitor array especially used in a high frequency field.

[0002]

[Description of the Prior Art] As shown in drawing 5 , the conventional penetration mold multilayer capacitor array sandwiches the dielectric sheet 31 which installed four penetration electrodes 32 in the front face side by side with the dielectric sheet 31 of two sheets which formed the grand electrode 34 in the front face, arranges the dielectric sheet for protective layers (not shown) in these vertical both sides further, and is taken as a layered product 36. In the front face of a layered product 36, as shown in drawing 6 , the signal external electrodes 38a-38d, 39a-39d, and the grand external electrodes 40 and 41 are formed, and it considers as the penetration mold multilayer capacitor array 43.

[0003] Drawing 7 is the electric representative circuit schematic of this capacitor array 43. With the grand electrode 34, each penetration electrode 32 constitutes four feedthrough capacitor components C1-C4. And these feedthrough capacitor components C1-C4 are arranged in the location equal to the direction of a laminating.

[0004]

[Problem(s) to be Solved by the Invention] If it is in the conventional capacitor array 43, it is easy to generate stray capacity Cs between the adjoining penetration electrodes 32, therefore easy to generate the electromagnetic compatibility between the penetration electrodes 32, and the so-called cross talk. In case a capacitor array is especially used in a RF field, the problem of a cross talk becomes remarkable.

[0005] As a cure of this cross talk, as shown in drawing 8 , spacing of the penetration electrode 32 can be secured enough, or as shown in drawing 9 , the cure of arranging the grand electrode 45 between the penetration electrodes 32 can be considered. However, if components size is the same, electrostatic capacity will become small, and if it is going to obtain the same capacity, there is fault that components size becomes large.

[0006] Then, the purpose of this invention has a cross talk between capacitor elements in offering a small mass penetration mold multilayer capacitor array few.

[0007]

[Means for Solving the Problem] In order to attain the above purpose, the penetration mold multilayer capacitor array concerning this invention is characterized by having arranged two or more penetration electrodes in a location which is different in the direction of a laminating, respectively, and changing the location of two or more feedthrough capacitor components in the direction of a laminating, respectively.

[0008]

[Function] By the above configuration, the arrangement location of a feedthrough capacitor component serves as different structure in the direction of a laminating, and the stray capacity which the grand electrode arranged in the penetration inter-electrode of each feedthrough capacitor component generates between penetration electrodes is stopped.

[0009]

[Embodiment of the Invention] Hereafter, 1 operation gestalt of the penetration mold multilayer capacitor array concerning this invention is explained with reference to an accompanying drawing. In addition, although this operation gestalt explains the thing equipped with four feedthrough capacitor components, it cannot be overemphasized that you may have two, three, or five feedthrough capacitor components or more in addition to this.

[0010] As shown in drawing 1 , the penetration mold multilayer capacitor array 1 consists of a dielectric sheet 2 which formed the penetration electrodes 4, 5, 6, and 7 in the front face, respectively, a dielectric sheet 2 which formed the grand electrodes 8, 9, 10, 11, and 12 in the front face, respectively, a dielectric sheet for protective layers (not shown), etc. Resin or ceramic dielectrics, such as epoxy, etc. are used as an ingredient of the dielectric sheet 2.

[0011] The penetration electrode 4 is formed in the front face of the dielectric sheet 2 at extensive area, and has the two cash-drawer sections 4a and 4b. Cash-drawer section 4a was exposed to the location on the right-hand side of the side of the near side of the dielectric sheet 2, and cash-drawer section 4b is

exposed to the location on the right-hand side of the side by the side of the back of a sheet 2. Similarly, the penetration electrode 5 was formed in the front face of the dielectric sheet 2 at extensive area, and exposed cash-drawer section 5a to the location of center-section rightist inclinations of the side of the near side of a sheet 2, and cash-drawer section 5b has exposed it to the location of center-section rightist inclinations of the side by the side of the back of a sheet 2. The penetration electrode 6 was formed in the front face of a sheet 2 at extensive area, and exposed cash-drawer section 6a to the location of the center-section left of the side of the near side of a sheet 2, and cash-drawer section 6b has exposed it to the location of the center-section left of the side by the side of the back of a sheet 2. The penetration electrode 7 was formed in the front face of a sheet 2 at extensive area, and exposed cash-drawer section 7a to the location on the left-hand side of the side of the near side of a sheet 2, and cash-drawer section 7b has exposed it to the location on the left-hand side of the side by the side of the back of a sheet 2. Although each penetration electrodes 4-7 are carrying out the same configuration, you may be a configuration which does not necessarily limit to this and is different.

[0012] The grand electrodes 8-12 were formed in the front face of the dielectric sheet 2 at extensive area, respectively, they exposed each cash-drawer section 8a, 9a, 10a, 11a, and 12a to the left part of a sheet 2, and the cash-drawer sections 8b, 9b, 10b, 11b, and 12b have exposed them to the right-hand side of a sheet 2. Electrodes 4-12 consist of ingredients, such as Ag-Pd, and Ag, Pd, Cu, and are formed by approaches, such as the sputtering method, a vacuum deposition method, and print processes.

[0013] After each dielectric sheet 2 accumulates by turns the dielectric sheet 2 which formed the penetration electrodes 4-7, respectively, and the dielectric sheet 2 which formed the grand electrodes 8-12, respectively, as shown in drawing 2 , let it be a layered product by arranging the dielectric sheet for protective layers in vertical both sides, and sintering in one. As shown in drawing 3 , the grand external electrodes 17 and 18 are formed in the lateral portion of

right and left of a layered product, the input external electrodes 15a, 15b, 15c, and 15d are formed in the lateral portion of a near side at equal intervals, and the output external electrodes 16a, 16b, 16c, and 16d are formed in the lateral portion by the side of the back at equal intervals. The external electrodes 15a-15d, 16a-16d, and 17 and 18 are formed by approaches, such as the sputtering method, a vacuum deposition method, and the applying method, and they consist of ingredients, such as Ag-Pd, and Ag, Pd, Cu.

[0014] The input external electrodes 15a-15d are electrically connected to the cash-drawer sections 4a-7a of the penetration electrodes 4-7, respectively, the output external electrodes 16a-16d are electrically connected to the cash-drawer sections 4b-7b of the penetration electrodes 4-7, respectively, and the external grand electrodes 17 and 18 are electrically connected to the cash-drawer sections 8a-12a of the grand electrodes 8-12, and 8b-12b, respectively.

[0015] In this way, the obtained capacitor array 1 constitutes the feedthrough capacitor component C1 from grand electrodes 8 and 9 and a penetration electrode 4, constitutes the feedthrough capacitor component C2 from grand electrodes 9 and 10 and a penetration electrode 5, constitutes the feedthrough capacitor component C3 from grand electrodes 10 and 11 and a penetration electrode 6, and constitutes the feedthrough capacitor component C4 from grand electrodes 11 and 12 and a penetration electrode 7. That is, the grand electrodes 9, 10, and 11 are shared by the adjoining feedthrough capacitor component. Drawing 4 is the electric representative circuit schematic of a capacitor array.

[0016] In this capacitor array 1, the penetration electrodes 4-7 are arranged in a different location in the direction of a laminating, i.e., the thickness direction of electrodes 4-7, and the feedthrough capacitor components C1-C4 have structure accumulated in the direction of a laminating. Since the grand electrode 9 is arranged among the penetration electrodes 4 and 5, the stray capacity generated between the penetration electrode 4 and 5 by this is stopped, and it is hard coming to generate the cross talk between the feedthrough capacitor components C [C1 and] 2. Similarly, the stray capacity generated between the

penetration electrode 5 and 6 is stopped with the grand electrode 10, and the cross talk between the feedthrough capacitor components C [C2 and] 3 stops being able to generate it easily. The stray capacity generated between the penetration electrode 6 and 7 is stopped with the grand electrode 11, and the cross talk between the feedthrough capacitor components C [C3 and] 4 stops being able to generate it easily.

[0017] Moreover, since it is the structure which carries out the laminating of the penetration electrodes 4-7 or the grand electrodes 8-12, only one electrode is arranged by the same layer, but these electrodes 4-12 can be set as extensive area, and mass electrostatic capacity is obtained. And spacing of the penetration electrode juxtaposed on the same dielectric sheet is secured enough, or since it is not the structure which arranges a grand electrode in the penetration inter-electrode juxtaposed on the same dielectric sheet, components size becomes small, and the area occupied to a printed circuit board etc. is small, and ends.

[0018] in addition, the penetration mold multilayer capacitor array concerning this invention is not limited to said operation gestalt, within the limits of the summary, can be boiled variously and can be changed. Although each feedthrough capacitor component of said operation gestalt consists of one penetration electrode and two grand electrodes, in order to enlarge electrostatic capacity, the number of sheets of a penetration electrode and a grand electrode may be increased. Moreover, although the adjoining feedthrough capacitor component is sharing the grand electrode, it may have the grand electrode which became independent for every feedthrough capacitor component.

[0019] furthermore, said operation gestalt -- an individual -- although the case of a product was made into the example and explained, it can manufacture with the mother substrate which equipped the case at the time of mass production with two or more capacitor arrays, it can start in desired size, and can consider as a product. Moreover, although said operation gestalt is calcinated in one after it accumulates a sheet, it is not necessarily limited to this. A sheet may use what was sintered beforehand. Moreover, the capacitor array which has a laminated

structure may be obtained by applying paste-like dielectric materials and a conductor ingredient to order, drying by approaches, such as printing, and giving two coats.

[0020]

[Effect of the Invention] Since the penetration electrode is arranged in a different location in the direction of a laminating by the above explanation according to this invention so that clearly, and the location of a feedthrough capacitor component was changed in the direction of a laminating, respectively, a grand electrode is arranged in the penetration inter-electrode arranged in the direction of a laminating, and the stray capacity which this grand electrode generates between penetration electrodes is reduced. Consequently, there are few cross talks between capacitor elements, and a small mass penetration mold multilayer capacitor array is obtained.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The decomposition perspective view showing 1 operation gestalt of the penetration mold multilayer capacitor array concerning this invention.

[Drawing 2] The perspective view showing the laminating condition of a penetration mold multilayer capacitor array shown in drawing 1 .

[Drawing 3] The perspective view showing the appearance of a penetration mold multilayer capacitor array shown in drawing 1 .

[Drawing 4] The electric representative circuit schematic of the penetration mold multilayer capacitor array shown in drawing 3 .

[Drawing 5] The decomposition perspective view of the conventional penetration mold multilayer capacitor array.

[Drawing 6] The perspective view showing the appearance of a penetration mold multilayer capacitor array shown in drawing 5 .

[Drawing 7] The electric representative circuit schematic of the penetration mold multilayer capacitor array shown in drawing 6 .

[Drawing 8] The perspective view showing the modification of the conventional penetration electrode layer.

[Drawing 9] The perspective view showing another modification of the conventional penetration electrode layer.

[Description of Notations]

1 -- Penetration mold multilayer capacitor array

2 -- Dielectric sheet

4, 5, 6, 7 -- Penetration electrode

8, 9, 10, 11, 12 -- Grand electrode

C1, C2, C3, C4 -- Feedthrough capacitor component

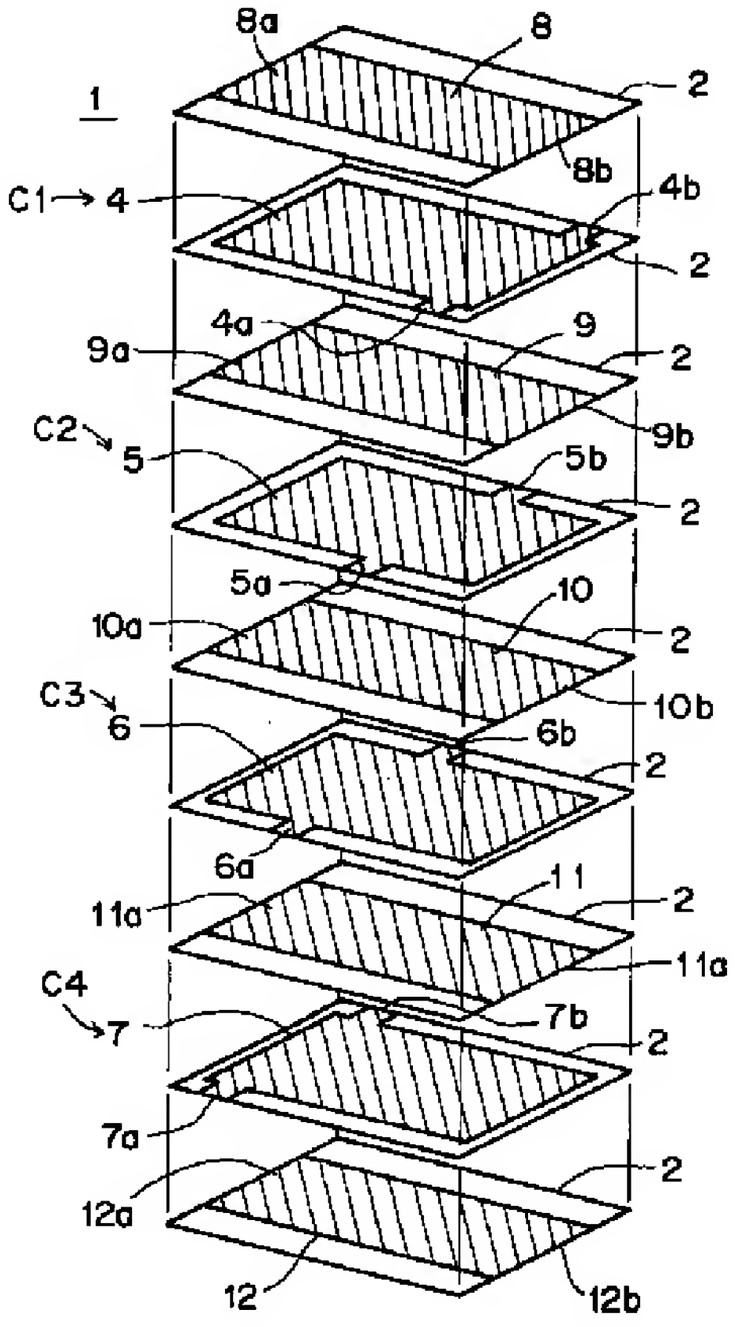
[Translation done.]

2.**** shows the word which can not be translated.

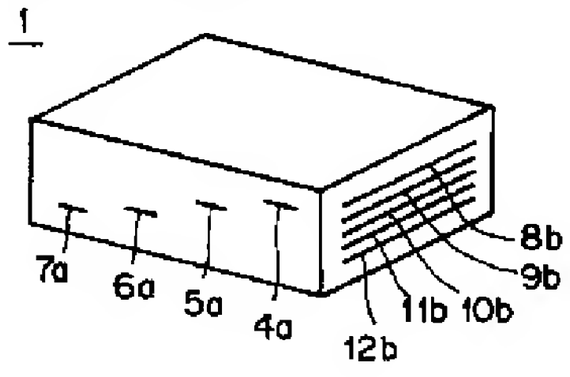
3.In the drawings, any words are not translated.

DRAWINGS

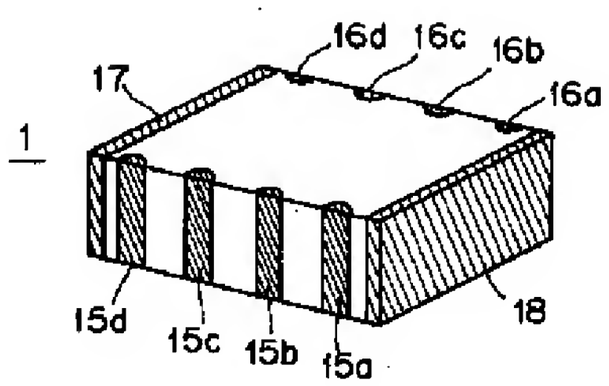
[Drawing 1]



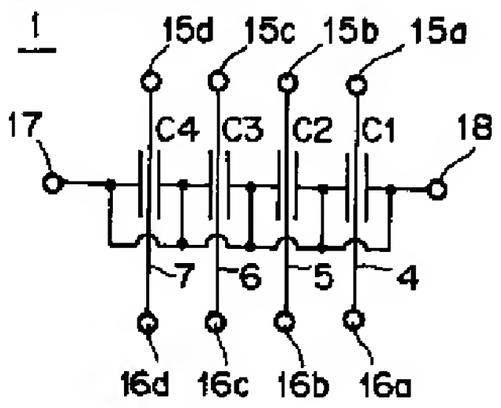
[Drawing 2]



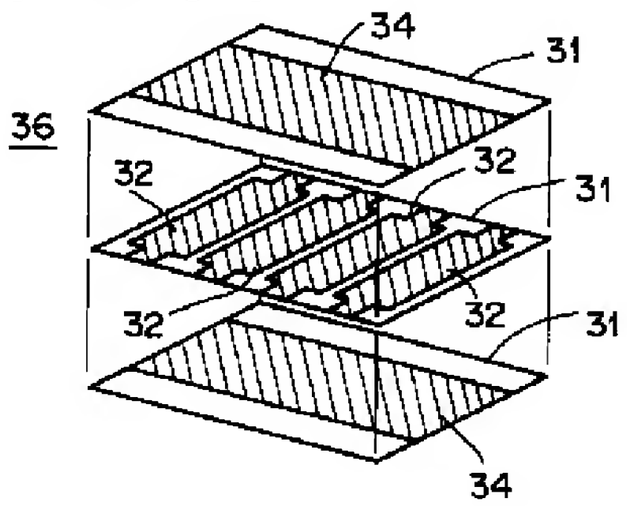
[Drawing 3]



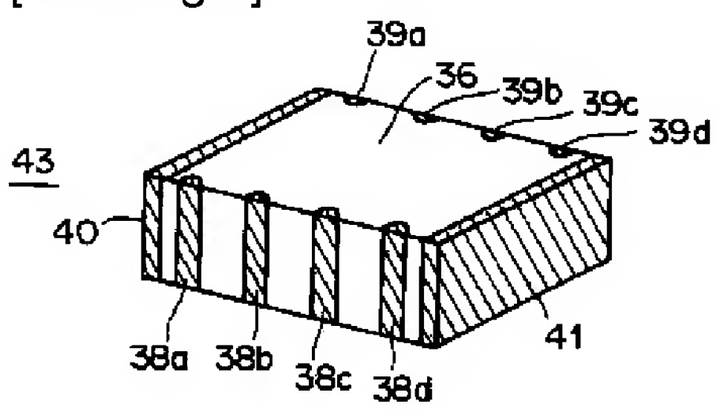
[Drawing 4]



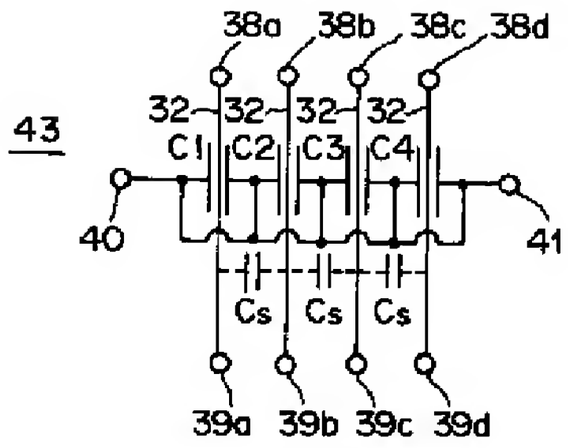
[Drawing 5]



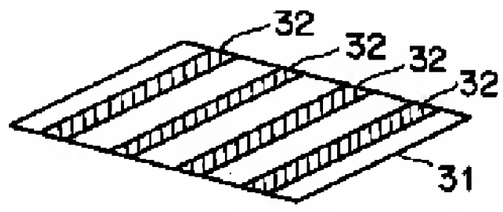
[Drawing 6]



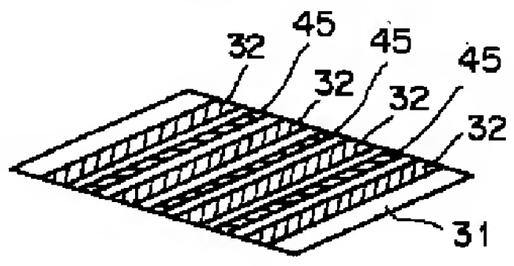
[Drawing 7]



[Drawing 8]



[Drawing 9]



[Translation done.]